

# DATA SHEET

## **74LVC38A**

Quad 2-input NAND gate (open drain)

Product specification  
Supersedes data of 2004 Mar 10

2004 Mar 22

## Quad 2-input NAND gate (open drain)

## 74LVC38A

## FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Open-drain outputs
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

## DESCRIPTION

The 74LVC38A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC38A provides the 2-input NAND function.

The outputs of the 74LVC38A devices are open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PZL}$	propagation delay nA, nB to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	1.7	ns
$t_{PLZ}$	propagation delay nA, nB to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.3	ns
$C_I$	input capacitance		4.0	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	5.5	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_i = \text{GND to } V_{CC}$ .

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC38AD	$-40$ to $+125$ °C	14	SO14	plastic	SOT108-1
74LVC38ADB	$-40$ to $+125$ °C	14	SSOP14	plastic	SOT337-1
74LVC38APW	$-40$ to $+125$ °C	14	TSSOP14	plastic	SOT402-1
74LVC38ABQ	$-40$ to $+125$ °C	14	DHVQFN14	plastic	SOT762-1

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**FUNCTION TABLE**

See note 1.

INPUTS		OUTPUTS
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

**Note**

- H = HIGH voltage level;  
L = LOW voltage level;  
Z = high-impedance OFF-state.

**PINNING**

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V <sub>CC</sub>	supply voltage

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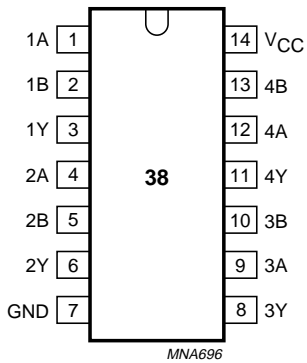
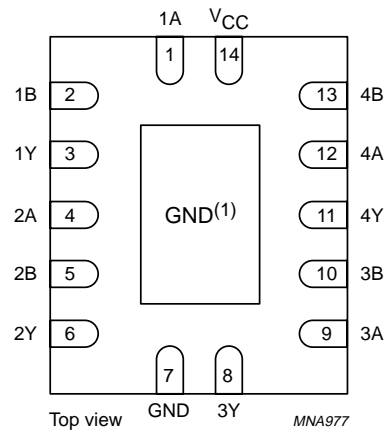


Fig.1 Pin configuration SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration (DHVQFN14).

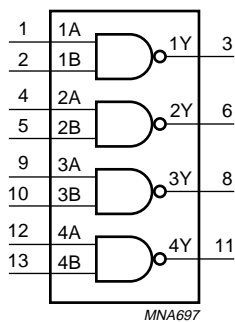


Fig.3 Logic symbol.

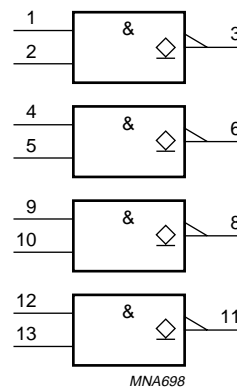


Fig.4 Logic symbol (IEEE/IEC).

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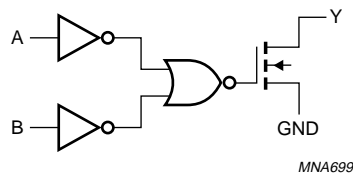


Fig.5 Logic diagram (one gate).

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage		0	5.5	V
$T_{amb}$	operating ambient temperature		-40	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.2$ to $2.7$ V	0	20	ns/V
		$V_{CC} = 2.7$ to $3.6$ V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O < 0$	-	-50	mA
$V_O$	output voltage	note 1	-0.5	+6.5	V
$I_O$	output sink current	$V_O = 0$ to $V_{CC}$	-	50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
For (T)SSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	-	GND	0.20	V
		I <sub>O</sub> = 100 μA	2.7	-	-	0.40	V
		I <sub>O</sub> = 12 mA	3.0	-	-	0.55	V
	I <sub>O</sub> = 24 mA						
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	±0.1	±5	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	5	500	μA
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	-	-	0.3	V
		I <sub>O</sub> = 100 μA	2.7	-	-	0.6	V
		I <sub>O</sub> = 12 mA	3.0	-	-	0.8	V
	I <sub>O</sub> = 24 mA						
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	-	±20	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	-	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	-	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	-	5000	μA

## Note

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PZL</sub>	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	5.7	–	ns
			2.7	0.5	1.7	2.9	ns
			3.0 to 3.6	0.5	1.7 <sup>(2)</sup>	3.0	ns
t <sub>PLZ</sub>	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	4.8	–	ns
			2.7	1.0	2.6	3.8	ns
			3.0 to 3.6	1.0	2.3 <sup>(2)</sup>	3.6	ns
t <sub>sk(0)</sub>	skew	note 3		–	–	1.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PZL</sub>	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	0.5	–	4.0	ns
			3.0 to 3.6	0.5	–	4.0	ns
t <sub>PLZ</sub>	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.0	–	5.0	ns
			3.0 to 3.6	1.0	–	4.5	ns
t <sub>sk(0)</sub>	skew	note 3		–	–	1.5	ns

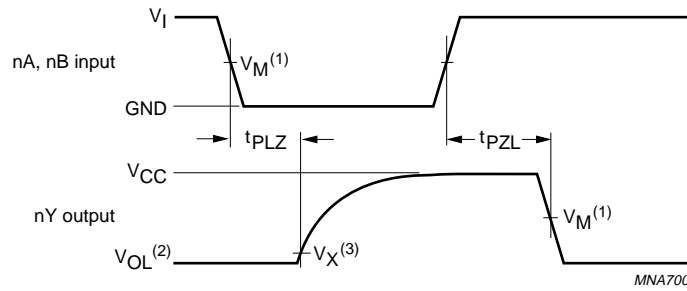
**Notes**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. These typical values are measured at V<sub>CC</sub> = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Quad 2-input NAND gate (open drain)

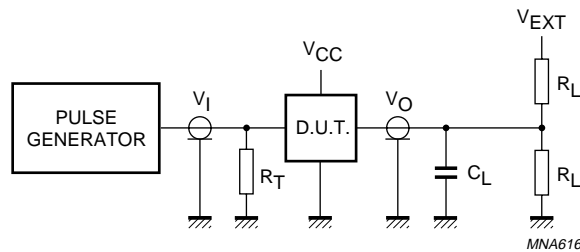
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AC WAVEFORMS



- (1)  $V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .  
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .
- (2)  $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.
- (3)  $V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .  
 $V_X = V_{OL} + 0.15\text{ V}$  at  $V_{CC} < 2.7\text{ V}$ .

Fig.6 The input nA, nB to output nY propagation delays.



V <sub>CC</sub>	V <sub>EXT</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>
1.2	2 × V <sub>CC</sub>	V <sub>CC</sub>	30 pF	500 Ω <sup>(1)</sup>
2.7	6 V	2.7 V	50 pF	500 Ω
3.3 to 3.6	6 V	2.7 V	50 pF	500 Ω

Note

- 1. The circuit performs better when  $R_L = 1000\ \Omega$ .

Definitions for test circuits:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$t_r = t_f \leq 2.5\text{ ns}$ ; when measuring  $f_{max}$ , there is no constraint on  $t_r$ ,  $t_f$  with 50% duty factor.

Fig.7 Load circuitry for switching times.



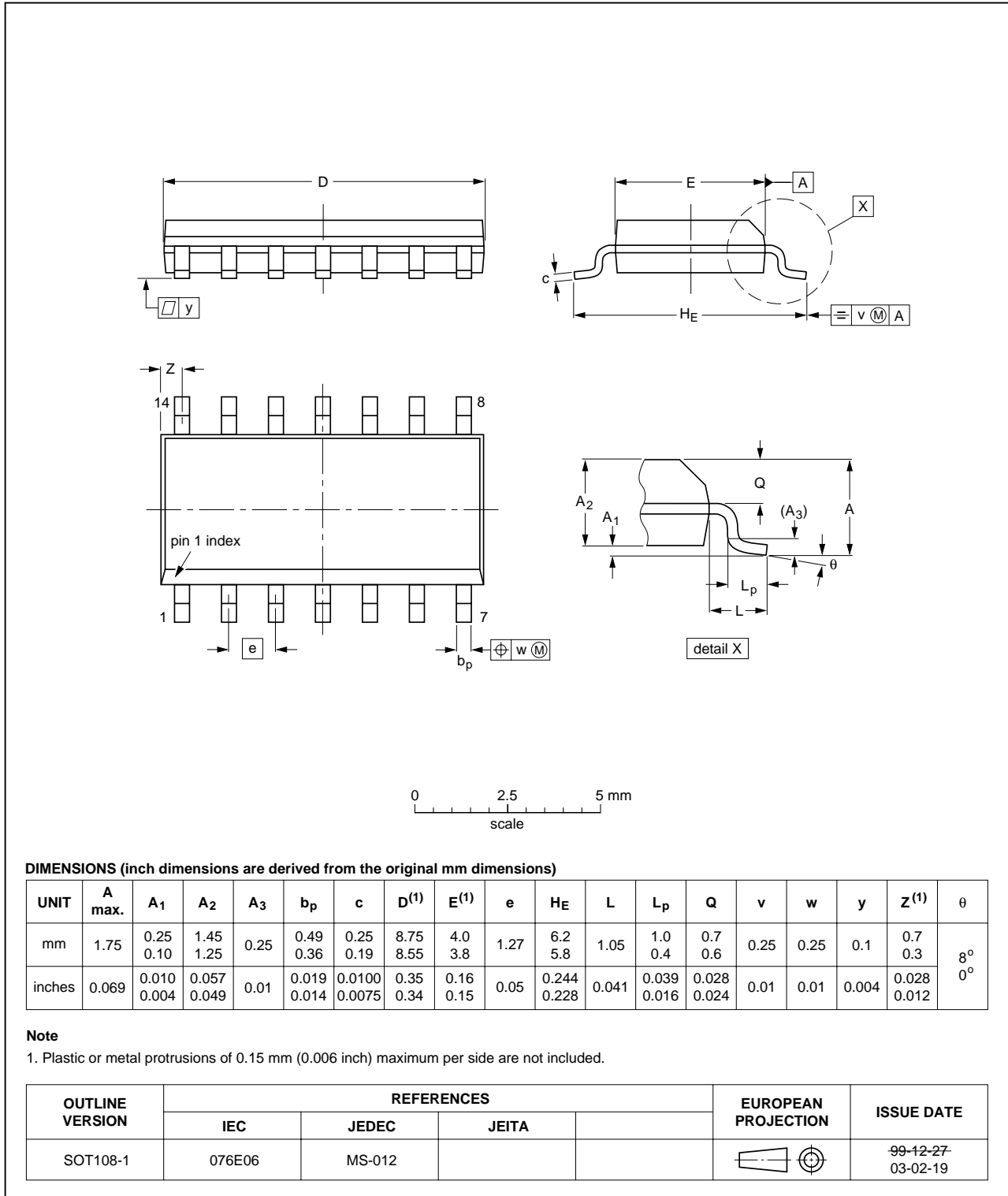
Quad 2-input NAND gate (open drain)

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PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

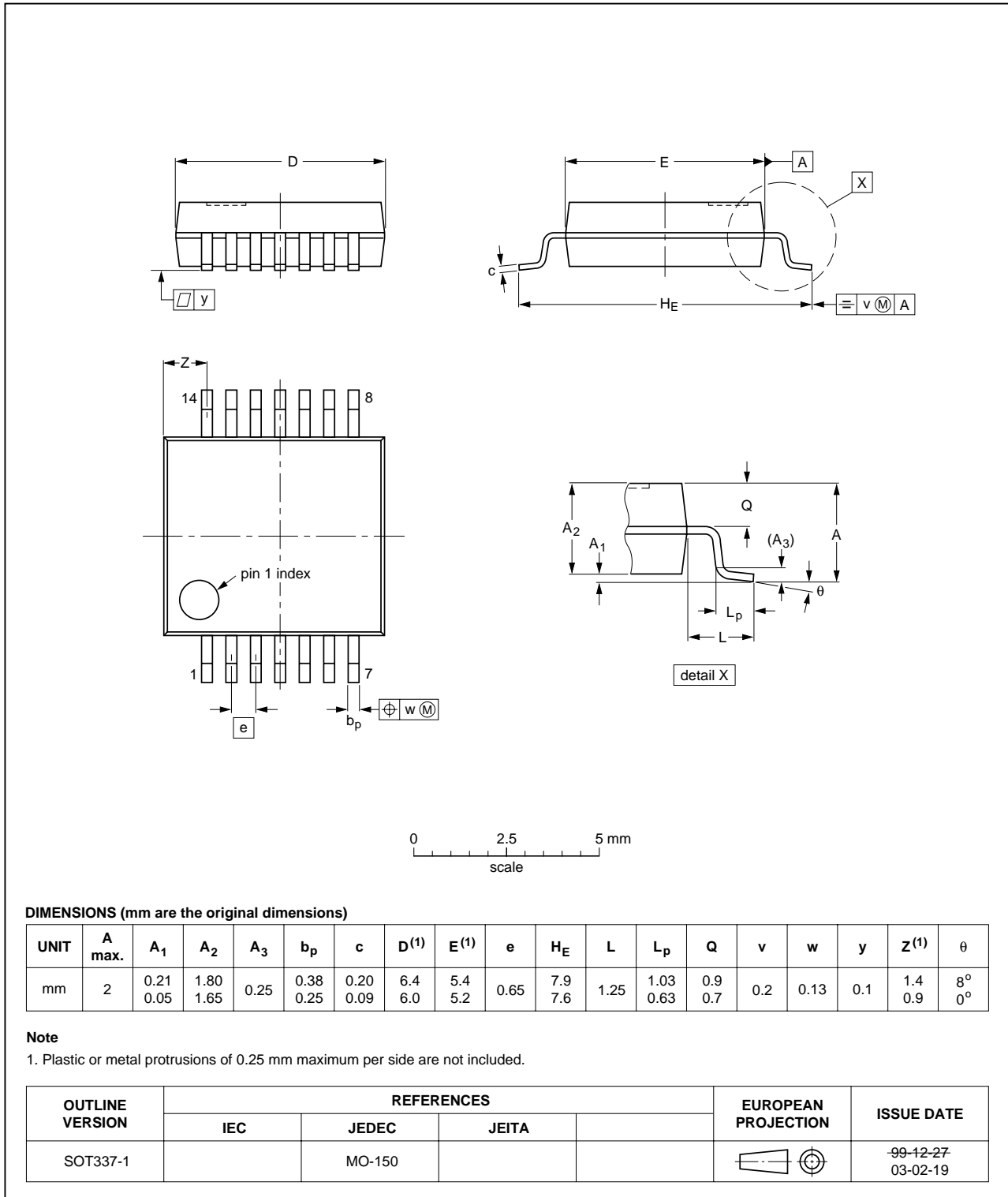


Quad 2-input NAND gate (open drain)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

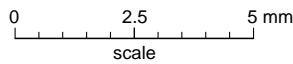
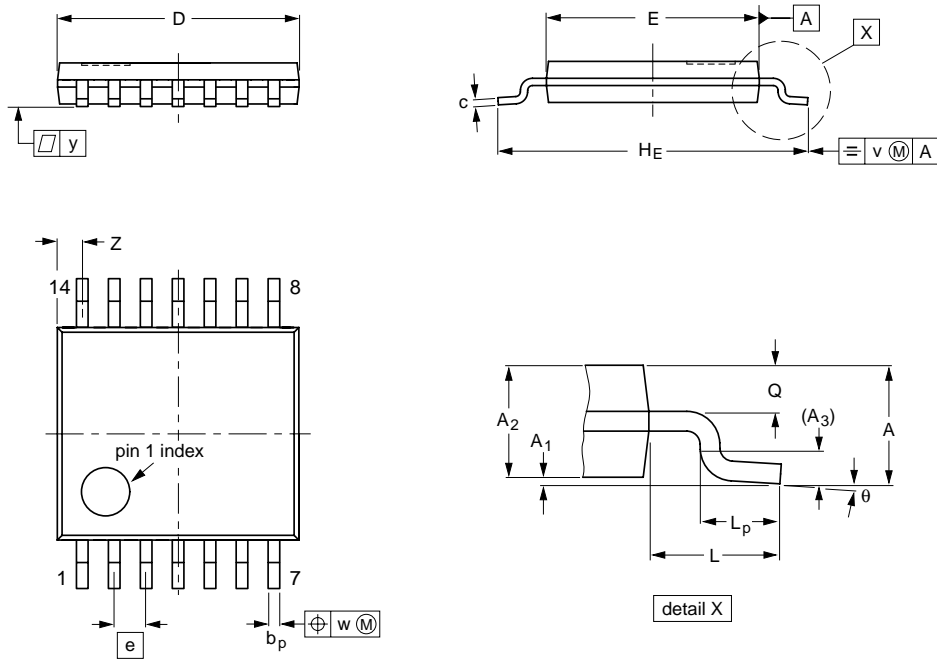


Quad 2-input NAND gate (open drain)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

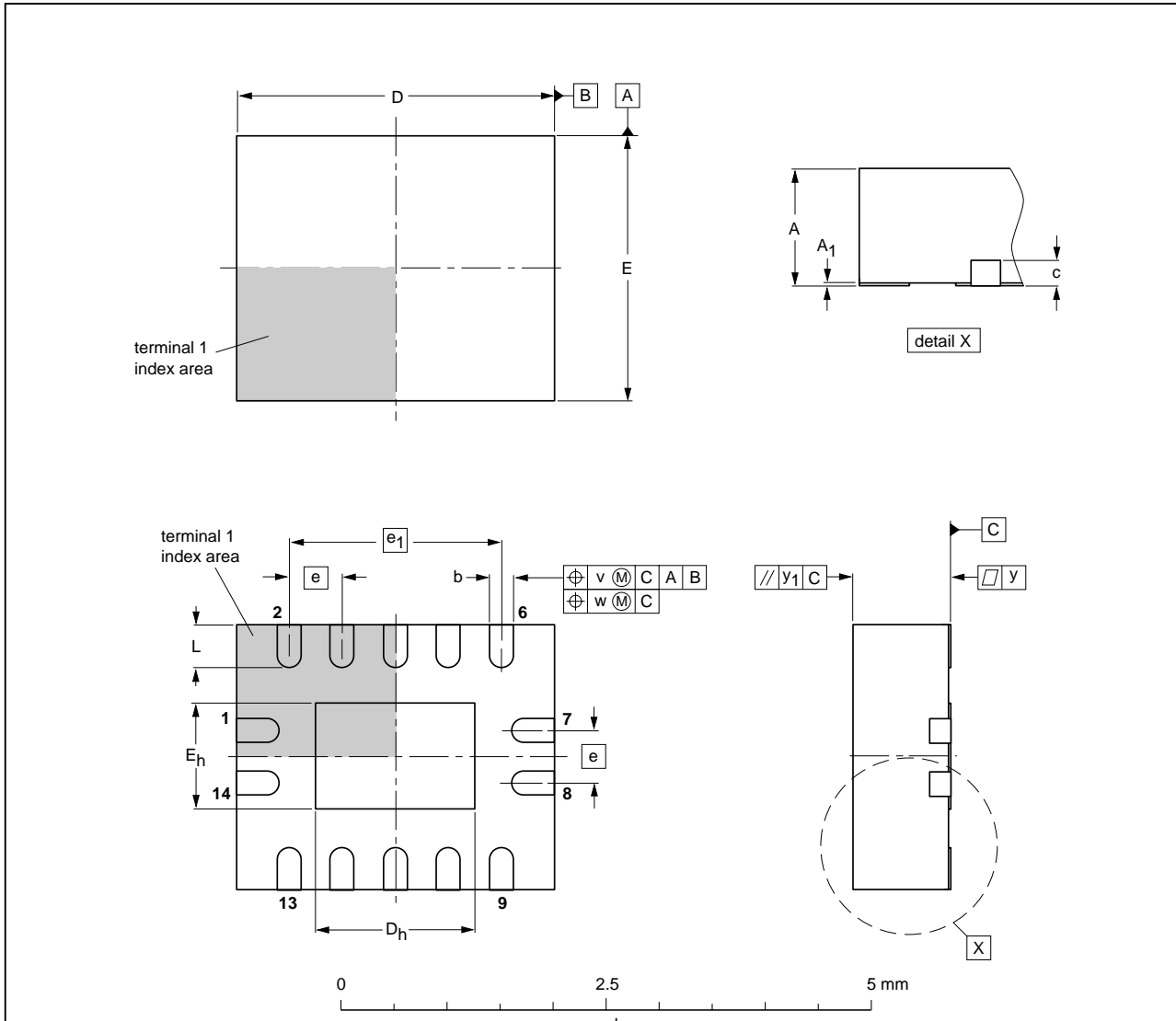
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT402-1		MO-153			99-12-27 03-02-18

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT762-1	---	MO-241	---		02-10-17 03-01-27

## Quad 2-input NAND gate (open drain)

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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